10710475

Electronic Version

Stylesheet Version v1.1.1

Description

Memory Module with Dynamic Termination Using Bus Switches Timed by Memory Clock and Chip Select

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of the co-pending application for "Trace-Impedance Matching at Junctions of Multi-Load Signal Traces to Eliminate Termination", U.S. Ser. No. 10/707,249, filed 12/1/2003, which is now a U.S. Patent 6,927,992 is a continuation-in-part of the co-pending application for "DDR Memory Modules With Input Buffers Driving Split Traces with Trace-Impedance Matching at Trace Junctions", U.S. Ser. No. 10/249,845, filed 5/12/03, which is now a U.S. Patent 6,947,304

BACKGROUND OF INVENTION

[0002] This invention relates to memory modules, and more particularly to dynamic, timed termination circuits.

[0003] Personal computers (PCs) and other electronic systems often use memory modules such as dual-inline memory